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A Novel Design Approach of Low Power Consuming Decoder using Reversible Logic Gates

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ABSTRACT

In current scenario, the reversible logic design is attracting more interest due to its low power consumption. Reversible logic is very important in low-power circuit design. The important reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate, toffoli gate, new gate and peres gate etc. Reversible Logic requires non-destruction of information. Therefore the number of inputs must be equal to the number of outputs. (If there were more outputs than inputs, the reverse direction wouldn't be reversible!). This paper presents a compact realization of quantum n-to-2n decoder circuit, where n is the number of input bits. The proposed design of the decoder circuit shows that it is composed of the quantum 2-to-4 decoder circuit. We present a decoder circuit using simple Feynman gate and tofolli gates. Designed circuit performs better than the existing ones, e.g., the proposed decoder circuit improves on the number of gates, delay, area and power. We simulated the circuit using cadence tool in both analog and digital.

Keywords: *Quantum Gate; Delay; Quantum Feynman and Tofolli Gates; Garbage Inputs and Outputs.*

1.0 Introduction

Most traditional computers lose information in the process of computation. Consider the simple two-input Boolean AND gate: Observing an output of 0 does not give enough information to identify the input combination that gave rise to the output. In fact, any one of three different input combinations (00, 01, 10) would force the output of the AND gate to 0. In computing the logical AND of two bits, a traditional AND gate would discard that input information. The only inherently logically reversible traditional primitives include the wire and inverter. The conclusions of Landauer and Bennett show that an energy loss of kTln2 joules in the form of heat unavoidably accompanies each bit of information discarded during computation, and that a completely reversible computer is theoretically possible. Only by performing the computation in a logically reversible manner can energy dissipation fall below kTln2 joules per bit per cycle. Decoders are a vital part of any modern digital computing device. They are used for addressing memories and caches, and they are used in conjunction with counters in multiphase clock generators. A decoder is a circuit that changes a code into a set of signals. It is called a decoder because it does the reverse of encoding, but we will begin our study of encoders and decoders with decoders because they are simpler to design. An n-to-2 n decoder takes an n bit input combination and asserts the output line addressed by that input combination. Each output line corresponds to exactly one input combination. Decoders can have an enable line, which functions as follows: If enable is activated, then the decoder's outputs behave as usual, that is, exactly one is activated at any time. If the enable input is not active, then all 2 n outputs of the decoder are deactivated. In this work we deal with reversible decoders without enable input.

Fig 1: (a) Implicit form of 2x4 Decoder

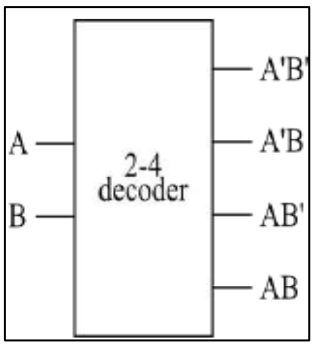

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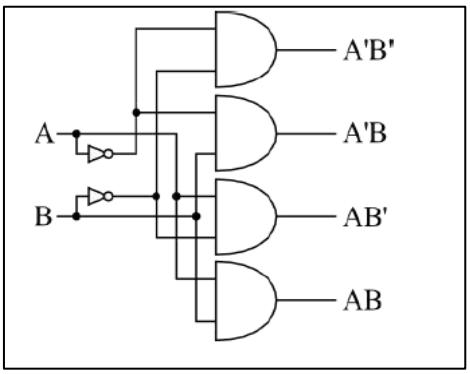
Fig1: (b) Schematic / Gate Level of 2x4 Decoder Circuit.



2.0 Basic Definitions

Most traditional logic gates, including the logical AND, OR, NAND, NOR, XOR, and XNOR gates, are irreversible. The observed output of any of these gates does not identify a unique input combination that causes that output. Researchers have developed several primitive reversible gates, including the Feynman, Toffoli, Fredkin, and Peres gates, and, in contrast to the basic gates of traditional logic, each possible output of any of these gates does uniquely identify the input combination that caused it [3, 4, 5].

In order to preserve information during computation, a reversible gate must operate in a way that effectively establishes a bijection between the set of input combinations and output combinations. That is, each input combination must identify a unique output combination (the gate computes an injective function), and each possible output combination must uniquely identify an input combination (this function is surjective).

This implies that reversible gates must have an equal number of inputs and outputs. Some gates, like the interaction gate [3], appear to violate this rule by having fewer inputs than outputs, but these gates still preserve information completely. The interaction gate can be considered to have four outputs, but it does not have 16 possible output combinations; it only has four, which equals the total number of input combinations.

A few metrics exist to compare reversible designs. The quantum cost of an implementation of a reversible circuit is equal to the number of quantum primitives the circuit uses. Here are few basic definitions to enlighten the reversible logic gates.

2.1. Reversible and fault tolerant gates:

An n × n reversible gate is a data stripe block that uniquely maps between input vector $I_v = (I_0 , I_1 , ..., I_{n-1})$ and output vector $O_v = (O_0 , O_1 , . . . , O_{n-1})$ denoted as $I_v \leftrightarrow O_v$.

Two prime requirements for the reversible logic circuit are as follows [14]:

- $I_0 \oplus I_1 \oplus ... \oplus I_{n-1} = O_0 \oplus O_1 \oplus ... \oplus O_{n-1}$
- There should be equal number of inputs and outputs.
- There should be one-to-one correspondence between inputs and outputs for all possible input-output sequences.

A Fault tolerant gate is a reversible gate that constantly preserves same parity between input and output vectors. More specifically, an n × n fault tolerant gate clarifies the Parity preserving property of Eq.1 allows to detect a faulty signal from the circuit's primary output. Researchers [11], [12], [15] have showed that the circuit consist of only re-versible fault tolerant gates preserves parity and thus able to detect the faulty signal at its primary output.

2.2 Qubit and quantum cost

The main difference between the qubits and conventional bits is that, qubits can form linear combination of states |0> or |1> called superposition, while the basic states |0> or |1> are an orthogonal basis of two-dimensional complex vector [3]. A superposition can be denoted as, $|\psi> = \alpha|0> + \beta|1>$, which means the probability of particle being measured in states 0 is $|\alpha|^2$, or results 1 with probability $|\beta|^2$, and of- course $|\alpha|^2 + |\beta|^2 = 1$ [16]. Thus, information stored by a qubit are different when given different α and β. Because of such properties, qubits can perform certain calculations exponentially faster than conventional bits. This is one of the main motivations behind the quantum computing. The quantum cost for all 1×1 and 2×2 reversible gates are considered as 0 and 1, respectively [6]~[14]. Hence, quantum cost of a reversible gate or circuit is the total number of 2 × 2 quantum gate used in that reversible gate or circuit.

2.2. Delay, garbage output and hardware complexity

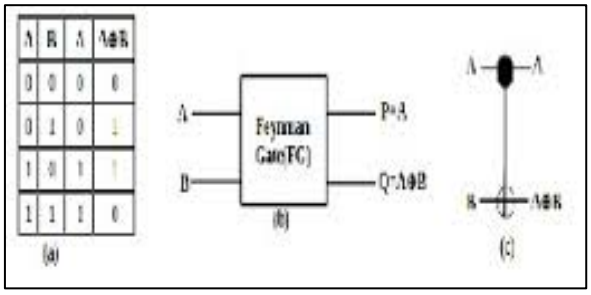
The delay of a circuit is the delay of the critical path. The path with maximum number of gates from any input to any output is the critical path [1]. There may be more than one critical path in a circuit and it

is an NP-complete problem to find all the critical paths [17]. So, researchers pick the path which is the most likely candidate for the critical paths [18].Unused output of a reversible gate (or circuit) is known as garbage output, i.e., the output which is needed only to maintain the reversibility are the garbage output.

2.4. Popular reversible fault tolerant gates:

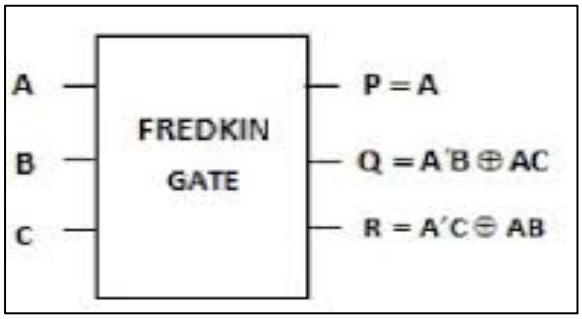
1) Let I_v and O_v are input and output vector of a 2*2 Feynman gate where I_v and O_v are defined as follows: I_v = (A, B) and O_v = (P = A, Q = A ^ B). The quantum cost of Feynman gate is 1. The block diagram and equivalent quantum representation for a 2*2 Feynman gate are shown in Fig. 2.

Fig 2 Operation and Quantum Circuit of Feynman Gate

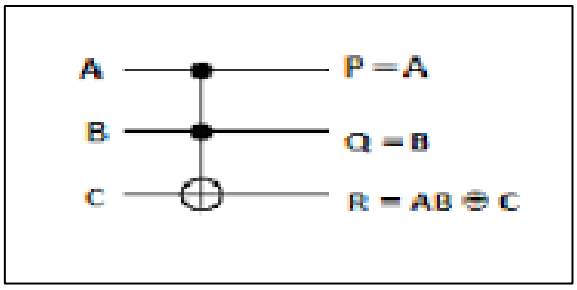


2) Fredkin Gate: The input and output vectors for 3 × 3 Fredkin gate (FDK) are defined as follows [20]: I_v = (a, b, c) and O_v = $^{(a,\ a'b \oplus ac,\ a'c \oplus ab)}$. Block diagram of FDK is shown in Fig. 3(a). Fig. 3(b) represents the quantum realization of FDK. In Fig. 3(b), each rectangle is equivalent to a 2 × 2 quantum primitive, therefore its quantum cost is considered as one [13]. Thus total quantum cost of FDK is five. To realize the FDK, four transistors are needed as shown

Fig 3(a) Operation Circuit of Feynman Gate



3(b) Operation and Quantum Circuit of Feynman Gate



3.0 Literature Survey

Enoch Hwang et all [4] showed that although power reduction techniques can be applied at every level of design abstraction, most automated power reduction techniques apply to the lower levels of design abstraction, such as the register-transfer or gate level.

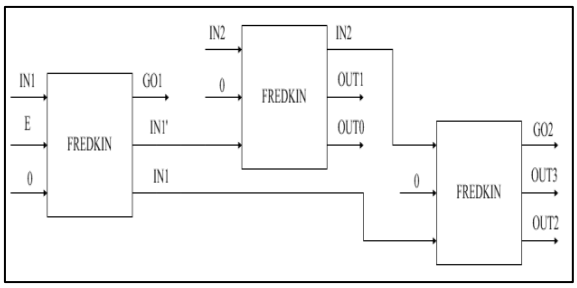
They have demonstrated through several experiments that functional partitioning, has already been shown to yield improvements in solving problems of I/O constraint satisfaction, synthesis complexity, and hardware/software partitioning, can also yield substantial reduction in power consumption (on average 41% total power reduction) with some overhead in size and performance. Yeong-Kang Lai, et al have showed [5] a new method for reversible variable length coding (RVLC) decoding. Alberto Nannarelli and Tomás Lang [6] have illustrated some techniques such as switching-off non active blocks, retiming, dual voltage, and equalizing the paths to reduce glitches for dividers realized in CMOS technology and energy dissipation reduction is carried out at different levels of abstraction: from the algorithm level down to the implementation or gate level.

Lafifa Jamal, et all [7] proposed the compact design of reversible circuits for a data acquisition and storage system. The design comprises with a compact reversible analog-to-digital converter and a reversible address register. In the way of designing this data acquisition and storage system they have proposed a reversible J-K flip-flop with asynchronous inputs, a reversible D flip-flop and a reversible three state buffer register. All the reversible designs individually have less number of gates, garbage outputs and quantum cost compared with the existing ones. S B Rashmi etall [8] proposed an improved design of a 4 x 4 multiplier using reversible logic gates. It is faster

and has lower hardware complexity compared to the existing designs. In addition, the proposed reversible multiplier is good in terms of number of gates, number of garbage outputs, number of constant inputs and quantum cost. Morrison et al [9] have proposed novel 4x4 RD gate implemented as a 2-to-4 decoder with low delay and cost, and a novel 4*4 R2D gate used in the implementation of a novel n-to-2 n decoder with low cost and delay.

A reversible synchronous up-down counter is presented and verified, and a reduced reversible implementation of a JK Flip Flop is implemented in a reduced reversible synchronous up-down counter. This decoder and counter are then utilized in the design of a reversible Moore finite state machine. Mozammel H. A. Khan [10] has shown the reversible realization of decoder multiplexer and de-multiplexer using quaternary reversible gates like quaternary shift gates (QSG), quaternary controlled shift gates (QCSG), and quaternary Toffoli gates (QTG). In [11], it is shown that it is possible to build sequential circuits with zero internal power dissipation. In [12] 2x4 decoder is realized using 3 Fredkin gates. The software used for simulation: XILINX and CADENCE.

Fig. 5 (a) 2x4 Decoder Using 3 FDK Gates

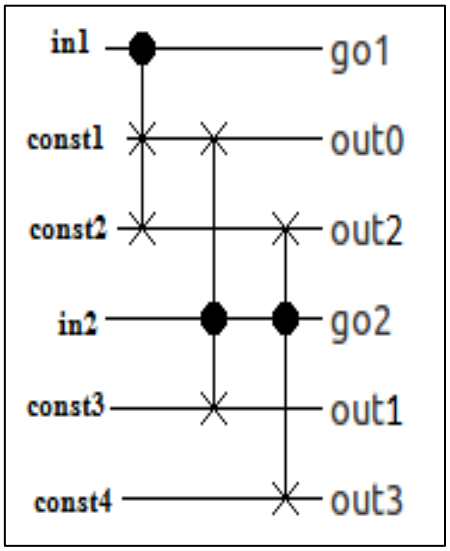


4.0 Design Flow

A conventional design symbol is as shown in the figure 5. The design requires totally 6 gates and area is around 80 um^2 with average power of 223.1nW. As they used three FDK gates, the total delay is more along with more power consumption.

As shown in figure 6 another conventional design is using one Feynman and two FDK gates which cover an area of 60 um^2 with average power of 96.94nW. The total delay is less than the conventional design but power consumption is still an issue

Fig 5(b) Circuit of Reversible Decoder using FDKs



The new design approach consists of two Feynman gates which has quantum cost of 1 each and four Toffoli gates which are of 3x3 dimensions. This design has all parameters satisfied when compared to conventional designs with more constant inputs and less garbage outputs. The parameter details are given in table 1.

The proposed design of a 2x4 Decoder requires 2 Feynman and 4 Toffoli Gates. This is as shown in Figure 8. This design requires a total of 6 gates. The total number of inputs is 8, which include 2 variable inputs and 6 constant inputs. Total number of outputs is 8, out of which 4 is garbage output. Constant inputs include 2 ones and 4 zeros.

The circuit symbol of 2x4 Decoder constructed using Feynman gates and Toffoli gates is shown in Figure 9.

Fig. 6 2x4 Decoder Using 1FEYNMAN & 2FDK Gates

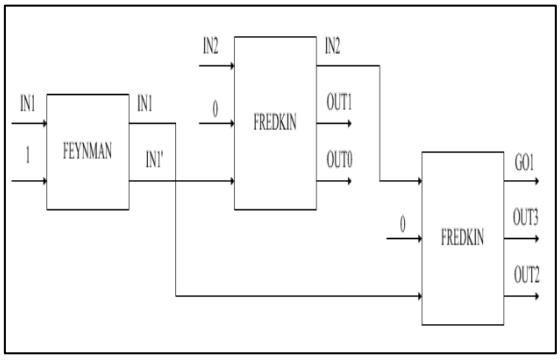
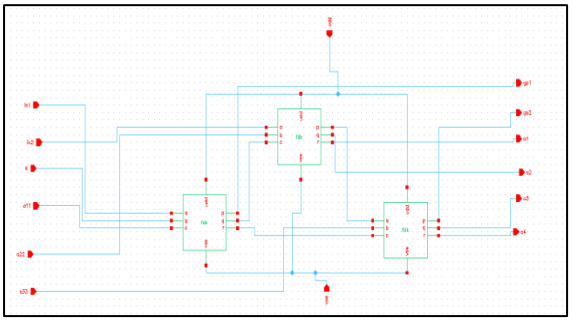


Fig.7 Schematic of Decoder Using 1FEYNMAN & 2FDK Gates



5.0 System Tools and Simulation

Figure 8: Circuit of Reversible Decoder using Feynman and Toffoli gates is shown. The a, b are the variable inputs, the constant inputs where the values of c and d are set to one and pins e, f, g, h are set to zero. For Feynman gate when one input is variable (that is 0 or 1) and other input is 1, the first output will be the variable input and the second output will be compliment of the first input. For Toffoli gate when the third input is zero the first two outputs will drive the first two

Fig 8: 2x4 Decoder Using 2FEYNMAN & 4 TOFFOLI Gates

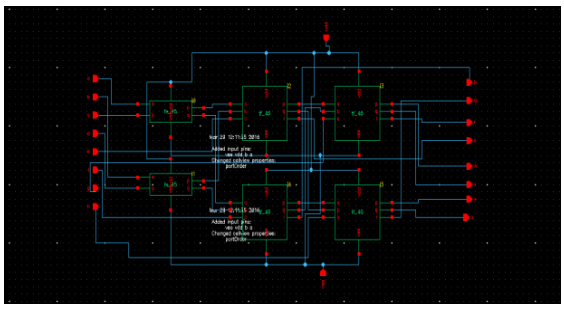


Fig 9:Symbol of Approached 2x4 Decoder using 1FEYNMAN & 2FDK Gates

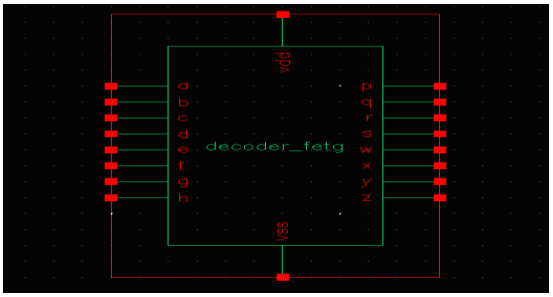


Fig. 10 Test Circuit for 2x4 Decoder using 1FEYNMAN & 2FDK Gates

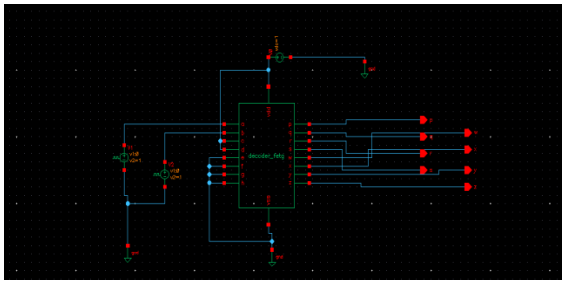
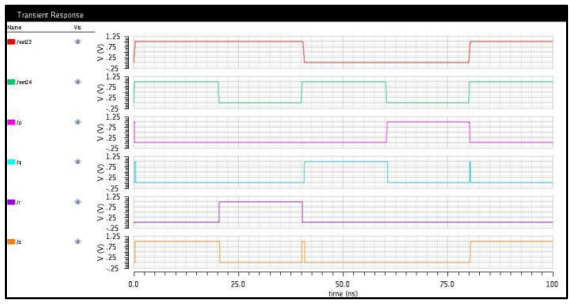


Fig 11 Output Waveforms of 2x4 Decoder



inputs and third output will be the AND product of first two inputs. The complete circuit is designed and verified in cadence virtuoso tool using 45nm technology. Fig 10 and 11 shows the test circuit and output waveform of the respective design.

5.1 Verilog hardware description language: It is most commonly used in the design and verification of digital circuits at the register-transfer level of abstraction. It is also used to verify of analog circuits and mixed-signal circuits. The complete project is designed using Verilog HDL language.

Fig 12: Power for 2x4 Decoder

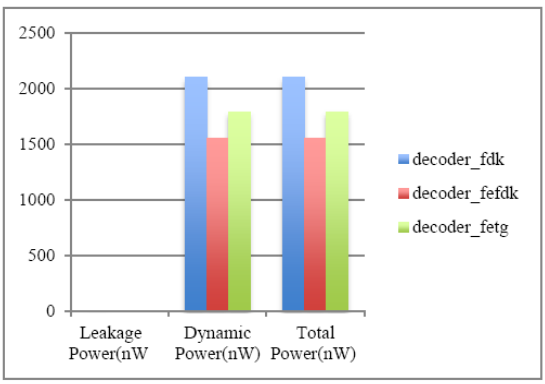


Table 1: Quantum Measurements

Design name	Delay (ps)	Total power (uw)	Area (u 2)	Gate coun t	Averag e power
Convention-al design	373	2102.8 44	80	6	223.1
Convention-al using Fe and FDK	219	1552.9 86	60	5	96.94
New design approach using Fe and Tg	209	1793.4 13	67	6	199.2

6.0 Analysis

Table I and Table 2 presents the quantum measurements for our reversible 2-to-4 decoder unit. Our design greatly improves over the conventional design of decoder using 3 Fredkin.

Gates in area power, delay. The improvements in these three metrics come at the cost of a slightly higher constant inputs and garbage outputs: The existing design has a quantum delay of 6, whereas our proposed design has a quantum delay of 6

Table 2.: Quantum Measurements for Decoder Unit

Design name	Total inputs	Constant inputs	Total outputs	Garbage outputs
Convention-al design	6	3	6	2
Convention-al using Fe and FDK	5	3	5	1
New design approach using Fe and Tg	8	6	8	4

7.0 Conclusion

Of all the reversible logical unit designs, notably little attention has been paid to the efficient implementation of reversible decoders. Quantum encoders and decoders, specifically designs of ternary and quaternary encoders and decoders, have been proposed, and a single binary reversible 2-to-4 decoder design has been proposed [10, 11, 12]. In this paper we propose a novel design of a reversible binary 2-to-4 decoder that realizes appreciable improvement over the existing reversible decoder design in three of four major metrics: quantum cost, garbage outputs and constant inputs. In fact, we achieve a 100% improvement in area, power consumption and delay over the existing design by eliminating them completely.

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